

REMARKS

Claims 1-21 are pending in this application. By this Amendment, claims 1, 3, 14, 16 and 18-20 are amended. Support for amended claims 1 and 14 may be found, for example, in paragraph [0012] in the instant application. No new matter is added. Reconsideration and allowance of the application is respectfully requested.

Allowable Subject Matter

Applicants appreciate that claims 9-13 and 21 are allowed; and claims 2-7 and 16-20 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the features of a base claim and any intervening claims. However, it is respectfully submitted that claims 1, 8 and 14-15 are also allowable in view of the foregoing amendments and the following remarks.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 8, 14, and 15 are rejected under 35 U.S.C. § 102(b) as being anticipated by Takaya, U.S. Patent 5,783,967. This rejection is respectfully traversed.

Applicants submit that Takaya fails to disclose or suggest, *inter alia*, "the control signal having a first voltage and a second voltage reflecting the detected phase difference", as recited in claim 1.

Takaya discloses in Fig. 2 a multiplier circuit having a first and second voltage control delay circuits 22, 23, a phase comparator 24 for comparing the phase of the input signal with the phase of an output signal of the second voltage control delay circuit 23, a loop filter circuit 25 responsive to the output signal of the phase comparator 24 for producing a control signal for controlling the first and second voltage control delay circuits 22, 23 to automatically correct a delay thereof such that an input signal passing through the first and second voltage control

delay circuits 23, 24 is delayed in phase by 180°, and an exclusive OR circuit 26 receptive of the input signal and the output signal of the first voltage control delay circuit 22 for outputting a double frequency output signal having a duty ratio of 50%.¹ However, Applicants submit that the control signal outputted from the phase comparator 24 of Takaya does not disclose or even mention of having a “first voltage” and a “second voltage” reflecting the detected phase difference.

As an example, non-limiting embodiment, Fig. 2 illustrates a first voltage V1 and a second voltage V2 outputted from the phase detector 231. The “voltages” may be used by the comparator 232 to compare the first voltage V1 and the second voltage V2, and outputted to a counter 233 to generate a logic signal having a predetermined logic state based on the result of the comparison. When the difference between the first voltage V1 and the second voltage V2 is greater than a predetermined value, the comparator 232 may output a signal for increasing the output signal of the counter 233. When the difference between the first voltage V1 and the second voltage V2 is less than the predetermined value, the comparator 232 may output a signal for decreasing the output signal of the counter 233.²

Accordingly, Takaya fails to disclose or suggest “the control signal having a first voltage and a second voltage reflecting the detected phase difference”, as recited in claim 1.

Accordingly, for at least these reasons, claim 1 and those claims dependent thereon are allowable over the applied art. Withdrawal of the rejection is respectfully requested.

Applicants further submit for the similar reasons as those stated above with regard to claim 1, that claim 14 and those claims dependent thereon are also allowable over the applied art. Withdrawal of the rejection is respectfully requested.

¹ See Takaya, col. 2, lines 26-35 and col. 3, lines 43-49

² See paragraph [0031] in the instant specification.

Accordingly, Applicants respectfully submit that for at least the reasons stated above, all currently pending claims 1-21 are now in condition for allowance. Withdrawal of any outstanding rejections and allowance of these claims are respectfully requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-21 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano, Reg. No. 35,094 at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By 
John A. Castellano, Reg. No. 35,094

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/DJC/